WHAT IS CLAIMED IS:

1. A method for fabricating a non-volatile memory device, the method comprising:

forming first and second vertical structures on first and second surface regions of a silicon substrate, each of the first and second vertical structures including a tunneling layer pattern, a charge trapping layer pattern, and blocking layer pattern sequentially stacked on the silicon substrate;

forming a gate insulating layer on a third surface region of the silicon substrate which is interposed between the first and second surface regions of the silicon substrate;

forming first and second gate spacers on respective surface portions of the gate insulating layer, the first gate spacer contacting an upper portion of a sidewall of the first vertical structure and protruding above an upper surface of the first vertical structure, and the second gate spacer contacting an upper portion of a sidewall of the second vertical structure and protruding above an upper surface of the second vertical structure;

forming a gate forming conductive layer on exposed surfaces of the first and second vertical structures, the first and second gate spacers, and the gate insulating layer;

etching the gate forming conductive layer to form first and second gate electrodes, wherein the first and second gate electrodes expose portions of the first and second vertical structures and the gate insulating layer;

removing the portions of the first and second vertical structures and the gate insulating layer exposed by the first and second gate electrodes by performing an etching process using the first and second gate electrodes as an etch mask; and

forming a source region and a drain region by implanting impurity ions in portions of the silicon substrate exposed by the first and second gate electrodes.

2. The method of claim 1, wherein forming the first and second vertical structures comprises:

sequentially stacking a tunneling layer, a charge trapping layer, and a blocking layer on the silicon substrate;

forming a mask layer pattern on the blocking layer which exposes a portion of the blocking layer; and

sequentially etching the blocking layer, the charge trapping layer, and the tunneling layer using the mask layer pattern as an etch mask to expose the third second surface region of the silicon substrate.

3. The method of claim 2, wherein the tunneling layer, the charge trapping layer, and the blocking layer are a first oxide layer, a nitride layer, and a second oxide layer, respectively.

4. The method of claim 3, wherein the first oxide layer is formed by thermal oxidation.

5. The method of claim 3, wherein the nitride layer is formed by one of low pressure chemical vapor deposition (LPCVD) or nitridation of the first oxide layer.

6. The method of claim 3, wherein the second oxide layer is formed by low pressure chemical vapor deposition (LPCVD).

7. The method of claim 2, wherein the mask layer pattern is a nitride layer pattern.

8. The method of claim 2, wherein the charge trapping layer is formed of a layer including polysilicon dots.

9. The method of claim 2, wherein the charge trapping layer is formed of a layer including nitride dots.

10. The method of claim 2, wherein forming the gate spacers comprises:

forming a gate spacer conductive layer on the gate insulating layer, the exposed sidewall of the vertical structure, and the mask layer pattern;

etching the gate spacer forming conductive layer to expose the mask layer pattern and the gate insulating layer; and

removing the mask layer pattern.

11. The method of claim 10, wherein the gate spacer forming conductive layer is a polysilicon layer.

12. The method of claim 1, wherein the gate forming conductive layer is formed using a polysilicon layer.

13. The method of claim 1, wherein the etching of the gate forming conductive layer is an etch-back process.

14. The method of claim 1, further comprising forming a metal silicide layer on the gate forming conductive layer.